2026 IEEE SNW
(Silicon Nanoelectronics Workshop)
June 13-14, 2026
Hilton Hawaiian Village, Honolulu, Hawaii

IEEE Electron Devices Society

A satellite conference of

2026 VLSI SYMPOSIUM

2026 IEEE Silicon Nanoelectronics Workshop

Advance Program

Day-1 Saturday June 13, 2026

Opening Remarks

Saturday June 13 8:30 AM

Peide Ye, Purdue University & Louis Hutin, CEA Leti

Session 1: Plenary Session

Saturday June 13 8:40 AM

Session Chair: Louis Hutin, CEA Leti

8:40 AM **1.1 *(Keynote)* Understanding of Carrier Transport Properties in Si Cryo-CMOS,** *S. Takagi[1,2], K. Sumita[2], Z. Jin[2], Y. Chen[2], H. Oka[3], T. Mori[3], M. Takenaka[2], and K. Toprasertpong[2], [1]Teikyo University, [2]The University of Tokyo, [3]National Institute of Advanced Industrial Science and Technology (AIST)*

Session 2: Cryogenic and Sensing Devices for Emerging Systems

Saturday June 13 9:15 AM

Session Chair: Pei-Wen Li, NYCU

9:15 AM **2.1 *(Invited)* Cryogenic CMOS Electronics at Millikelvin Temperatures for Quantum Computing Systems**, *A. Grill[1] , A. Potocnik[1] , A. C¸ aglar[1] , L. Fallik[1,2] , R. Acharya[1], R. Asanovski[1], E. Catapano[1], S. Van Winckel[1], S. Balamurali[1], C. Godfrin[1], B. Raes[1], J. van Staveren[1], I. Fattal[1,2], C. Dimri[1,2], J. Van Damme[1], A. Chasin[1], B. Kaczer[1], D. Wan[1], K. De Greve[1], [1]imec, [2]KU Leuven*

9:40 AM **2.2 Ultra-Scaled Cryogenic Ferroelectric Field-Effect Transistor with Highly Reliable Multi-Level Operation,** *Z. Lin[1], C. Niu[1], J.-Y. Lin[1], P.-K. Hsu[2], H. Dou[3], K. Xu[3], H. Wang[3], S. Yu[2], Peide D. Ye[1], [1]Purdue University (Electrical and Computer Engineering), [2]Georgia Institute of Technology, [3]Purdue University (Materials Engineering)*

9:55 AM **2.3 High-responsivity Ge Quantum-dot photoFinFET For Low Optical-power Detection,** *H. –H. Y. Cheng, C. –C. Liu, S. –H. Yang, H. –C. Lin, and P. –W. Li, National Yang Ming Chiao Tung University*

10:10 AM **2.4 A Novel AsyFET-based 2T Active Pixel Sensor for AI Glasses Image Sensors,** *K. Wang[1], Y. Zhu[1], X. Guo[1], Y. Yu[1], M. He[1], Q. Huang[1,2], R. Huang[1,2], [1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits*

Coffee Break 10:25 AM – 10:45 AM

Session 3: Oxide-Semiconductor Device Physics and Reliability

Saturday June 13 10:45 AM

Session Chair: Byoung Hun Lee, POSTECH

10:45 AM	**3.1 *(Invited)* Understanding Bias Temperature Instability in ITO Transistors,** *T. Roy, A. Sarkar, M. S. Rahman, and D. Matthews, Duke University*
11:10 AM	**3.2 *(Invited)* Bulk and Interfacial Defect Characterization and Suppression for High-Performance Top-Gate Oxide Semiconductor Transistors,** *M. Si, K. Jiang, and Z. Lin, Shanghai Jiao Tong University*
11:35 AM	**3.3 First Direct Measurement of Quantum Capacitance in Oxide Semiconductors Using Electric-Field-Penetration Technique,** *K. Nam[1], C. Niu[1], A. Shankar[1], J. -Yu Lin[1], S. Khare[1], S. Lee[1], J. Lu[2], C. Liu[2], H. Wang[1,2], P. Upadhyaya[1], Peide D. Ye[1], [1]Purdue University (Electrical and Computer Engineering), [2]Purdue University (Materials Engineering)*

Lunch Break 11:50 AM – 1:00 PM

Session 4: Memory-Centric Computing

Saturday June 13 1:00 PM

Session Chair: Takahiro Shinada, Tohoku University

1:00 PM	**4.1 *(Invited)* In-Memory Computing Approaches for Trustworthy AI: From Bayesian Methods to On-Chip Learning,** *E. Vianello[1], T. Januel[1], M. Piccoli[1], T. Hirtzlin[1], F. Rummens[2], T. Dalgaty[2], E. Hardy[1], M. Ezzadeen[1], J. Minguet Lopez[1], O. Billoint[1], L. Grenouillet[1], J.-M. Portal[3], L. Hutin[1], D. Querlioz[4], [1]CEA-Leti, University of Grenoble Alpes, [2]CEA-List, University of. Grenoble Alpes, [3]Aix Marseille University, [4]University of Paris-Saclay*
1:25 PM	**4.2 *(Invited)* Memristor / CMOS Integration for Neuro-inspired Computing Testbed,** *I. Hossen[1], O. Yousuf[1,2], M. Lueker-Boden[2], W. Borders[3], A. M.[3], G. Adam[1], [1]George Washington University, [2]Western Digital Research Center, [3] National Institute of Standards and Technology*
1:50 PM	**4.3 First Experimental Demonstration of Dual-layer Cross-Point Ferroelectric Capacitor Array based TCAM for Hyperdimensional Computing,** *Z. Zhang[1], H. Zheng[1], S. Cao[1], J. Zhu[1], W. Xu[1], Z. Fu[2], Q. Huang[1,3], and R. Huang[1,3], [1]Peking University, [2]Southeast University, [3]Beijing Advanced Innovation Center for Integrated Circuits*
2:05 PM	**4.4 Novel Gate-Injected Ferroelectric Memcapacitor with Capacitance-Clamping Enabling Op-Amp-Free Computing-in-Memory with Enhanced Linearity and Energy Efficiency for LLMs,** *B. Song[1], S. Xu[1], H. Wang[1], J. Luo[1], Q. Huang[1,2], R. Huang[1,2], [1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits*
2:20 PM	**4.5 A Novel TiN/TiO_2/HfOx/TiO_2/TiN Bi-directional Self-Rectifying Memristor for High Area-efficiency Video Compression,** *H. Ai[1,2], L. Wu[1,2], G. Li[1,2], Y. Chen[1,2], S. Li[1,2], Y. Feng[3], L. Liu[1,2], P. Huang[1,2], [1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits, [3]Beijing Information Science and Technology University*

Session 5: Dense and Embedded Memory Technologies I

Saturday June 13 2:35 PM

Session Chair: TBD

2:35 PM	**5.1 A Novel CMOS-Compatible 3T1C Embedded DRAM Structure for Multi-Gb On-Chip RAM in the AI Computing Era,** *H. –T. Lue, T. –H. Yeh, K.-C. Wang, and C.-Y. Lu, Macronix International Co., Ltd.*
2:50 PM	**5.2 System–Technology Co-Optimization of Bitline Routing and Bonding Pathways in Monolithic 3D DRAM Architectures,** *K. Lee, S. Cho, S. Lim, S. Datta, and S. Yu, Georgia Institute of Technology*
3:05 PM	**5.3 A 7-Å Double-CFET 4T-SRAM Architecture with 0.0053-μm^2 Cell Size for Overcoming the SRAM Memory Wall,** *H. L. Tsai[1], C. Y. Tsai[1], H. W. Chiu[1], Y.-Y. Chuang[1], M. –T. Kuo[1], and E. R. Hsieh[2], [1]National Central University, [2] National Yang Ming Chiao Tung University*

3:20 PM **5.4 A High-Precision Optimal Read Offsets (ORO) Prediction Approach for +300% Readable Cycles Enhancement in 3D QLC Flash Memory,** *X. Zhao[1] , J. Zhong[3], P. Wang[4] , M. Zhang[2], G. Wang[1], X. Zhan[1], F. Wu[2], J. Chen[1], [1]Shandong Univ., [2]Huazhong University of Science and Technology, [3]Jinan Maiwei Intelligent Technology Co., Ltd., [4]Shandong Sinochip Semiconductors Co. Ltd.*

Short Break 3:35-3:40 PM

Session 6: Ferroelectric Memories

Saturday June 13 3:40 PM

Session Chair: Minoru Oda, Kioxia

3:40 PM **6.1 *(Invited)* Ferroelectric Platforms for Advanced Non-Volatile Memory Technologies,** *X. Gong, X. Wang, Y. Feng, Z. Zhou, J. Xie, C. Sun, and L. Jiao, National University of Singapore (NUS), Singapore*

4:05 PM **6.2 Barrier-Engineered Fast Polarization Switching in Ferroelectric HZO Films by Atomic-Scale Doping: From First-Principles to Device Demonstration,** *X. Li[1,2], X. Zhao[2], P. Guo[3], X. Dou[2], Y. Feng[2], P. Sang[2], X. Zhan[2], J. Wu[2], D. Loke[1], and J. Chen[2], [1]Singapore University of Technology and Design, [2]Shandong University, [3]Shandong Sinochip Semiconductors Co. Ltd.*

4:20 PM **6.3 Unveiling Underlying Mechanism of Fatigue in HfO_2-Based Ferroelectric Films: Imprint as the Origin of Fatigue,** *Z. Liu[1], M. Takenaka[1], S. Takagi[1,2], K. Toprasertpong[1], [1]The University of Tokyo, [2]Teikyo University*

4:35 PM **6.4 Experimental Investigations on Read Instabilities in Ferroelectric HZO MFM: Defects' Dynamic Behaviors and A Proposal of Anti-Fatigue Readout Strategy,** *Y. Fan[1], X. Li[1], P. Wang[2], Y. Feng[1], P. Sang[1], X. Zhan[1], J. Wu[1], J. Chen[1], [1]Shandong University, [2]Shandong Sinochip Semiconductors Co. Ltd.*

Coffee Break 4:50 PM – 5:10 PM

Poster Session 1

Saturday June 13 5:10 PM – 7:00 PM

5:10 PM **Poster Introductions** (2 minutes each)

Session Co-Chairs: Steve Chung, NYCU, and K. S. Chang-Liao, NTHU

(Poster listings at the end)

Day-2 Sunday June 14, 2026

Session 7: Keynote

Sunday June 14 8:30 AM

Session Chair: Louis Hutin, CEA Leti

8:30 AM **7.1 *(Keynote)* Intelligent Memory: Enabling a Sustainable, Energy-Efficient Computing Future,** *T. –H. (Alex) Hou, National Yang Ming Chiao Tung University*

Session 8: Advanced CMOS Devices and Integration Technologies

Sunday June 14 9:05 AM

Session Chair: Katsuhiro Tomioka, Hokkaido University

9:05 AM **8.1 Design of HfO_2 Crystal Gate Stack for Enhancement of MOSFET Performance Studied by Calculation of Remote Phonon Scattering,** *T. Kawanago[1,2], T. Kamioka[1,2], Y. Morita[1,2], N. Okada[1,2], K. Manabe[1,2], W. Mizubayashi[1,2], H. Ota[1,2], Takashi Matsukawa[1,2], and Shinji Migita[1,2], [1]AIST, [2]LSTC*

9:20 AM **8.2 Critical Chip-Level Examination on GAA Technology with Dual-sided Interconnects from BSPDN to Backside Clock: Architecture Innovations, PPA and First Signal/Power Integrity Analysis,** *F. Teng[1], X. Yan[1], W. Peng[1], J. Sun[1], H. Lu[1], Y. Chu[1], M. Lin[1], C. Zhou[1], X. Jiang[1], X. Li[1], J. Jin[1], K. Guo[1], Z. Jin[2], C. Zhuo[2], Y. Lin[1], R. Wang[1], M. Li[1], H. Wu[1], [1]Peking University, [2]Zhejiang University*

9:35 AM **8.3 Alloy and Nitridation of Gate Dielectric Stack on Electrical and Reliability Characteristics of RG-FinFETs for 1T4R 3D RRAM,** *Y. –R. Lin[1], K.-S. Chang-Liao[1,2], S. S. Chung[3], [1]National Tsing Hua University, [2]National Tsing Hua University, [3]National Yang Ming Chiao Tung University*

Coffee Break 9:50 AM – 10:10 AM

Session 9: Ferroelectric Memory Reliability

Sunday June 14 10:10 AM

Session Chair: Masaharu Kobayashi, The University of Tokyo

10:10 AM **9.1 Frequency-dependent Field Cycling for Imprint Recovery in Ultra-thin $Hf_{0.5}Zr_{0.5}O_2$ Ferroelectric Capacitors,** *T. Liu[1], Z. Liu[1], K. Ito[1], Z. Jin[1], S. Takagi[2], M. Takenaka[1], K. Toprasertpong[1], [1]The University of Tokyo, [2]Teikyo University*

10:25 AM **9.2 Investigation of Breakdown Acceleration in HfO_2-based Ferroelectric Capacitors after Low-Field Fatigue Cycles,** *K. Sun[1], H. Li[2], Z. Shang[2], L. Zeng[1], M. Li[2], and R. Wang[2], [1]Beihang University, [2]Peking University*

10:40 AM **9.3 Thermally Activated Relaxation of Non-Accumulative Write Disturb with a Tens-of-Nanoseconds Critical Interval in 3D Oxide-Channel FeFETs,** *M. Yu[1], Y. Zhou[1], R. Zhu[1], X. Xu[1], R. Huang[1,2], and K. Tang[1,2], [1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits*

Session 10: Dense and Embedded Memory Technologies II

Sunday June 14 10:55 AM

Session Chair: Jiezhi Chen, Shandong University

10:55 AM **10.1 Physical Analysis and Experimental Optimization of Vertical 3D Stack-ability of Hafnia-based 0TnC FeRAM for High-density Memory Applications,** *M. Deng[1], S. Cao[1], L. Zou[1], Q. Huang[1,2,3], and R. Huang[1,2,3], [1]Peking University, [2]Beijing Advanced Innovation Center for Integrated Circuits, [3]Beijing Superstring Academy of Memory Technology*

11:10 AM **10.2 A 16-nm Non-Volatile 4-T-1-FeCap SRAM with 0.17 fJ/b Write-Energy and 0.033 μm^2 Cell Area,** *K. –W. Cheng[1], C. –Y. Lin[2], T. –W. Liu[2], and E. R. Hsieh[1], [1]National Yang Ming Chiao Tung University, [2]National Central University*

11:25 AM **10.3 A Hafnia-based Fusion FeRAM with Integrated 1T1C and 1TnC Architecture for High-Speed In-Array KV Cache Transfer in Edge LLM Inference,** *Y. Z.[1], Y. Shen[1], X. Zhang[1], J. Su[1], H. Cai[1,2], Z. Fu[1,2], J. Yang[1,2], [1]Southeast University, [2]National Center of Technology Innovation for EDA*

Closing Remarks

11:40 AM **Announcement of 2027 SNW** — *Daniel Moraru, General Chair*

Poster Session papers

Saturday June 13 5:10 PM – 7:00 PM

5:10 PM **Poster Introductions** (2 minutes brief each)

[each presenter has the printed poster setup between 3:30-5:00]

P1-1 **First All-2D-Transistor-Driven BEOL Memory Vertical Integration of RRAM and Gain-Cell DRAM**, *N. Yang[1], W. Dang[3], C. Yao[2], W. Wei[3], Y.-M. Chang[1,2], F. Zheng[4], C. Li[1,2,] W. Li[2], Y. Wan[2], F. Miao[3], Y.-W. Lan[5], J.-K. Huang[1], S.-J. Liang[3] and L.-J. Li[1,2,5], [1]Nexstrom Pte. Ltd., [2]National University of Singapore, [3]Nanjing University, [4]The University of Hong Kong, [5]National Taiwan Normal University*

1-2 **A Monolithic 3-D Integrated Reconfigurable CMOS-NEM Threshold Logic Gate with Intrinsic Sign-Encoding for Energy-Efficient Computing**, *S. J. Kim[1,2], J. W. Lee[1], M. S. Shin[1], W. Y. Choi[1], [1]Seoul National University, [2]Samsung Electronics Co. Ltd*

P1-3 **A Configurable Analog In-Memory Computing Evaluation Framework for Transformer-based Large Language Model Inference,** *M. Choi[1], J. Lee[1], S. Kim[2] and W. Shim[1], [1]Seoul National University of Science and Technology, [2]Dongguk University*

P1-4 **Confirming Neuron Operation with MOSFET-Connected PN-Body Tied SOI-FET – Investigating High Input Impedance for Multi Neuron Connection,** *Y. Yamazaki[1], H. Yonezaki[1,2], J. Ida[1], and T. Mori[1], [1]Kanazawa Institute of Technology, [2]KIOXIA Corporation*

P1-5 **Potential of a Multiple-Electron Random Network for Reservoir Computing**, *S. Watanabe[1], T. Oya[1,2], [1]Yokohama National University, [2]Yokohama National University*

P1-6 **Amorphous-Si Nanoheater Enabled Stabilization of TaOx RRAM for High-Precision Analog In-Memory Computing,** *K. Beom[1], S. S. Swain[2], E. Stringer[1], M. A. Islam[1], A. A. Talin[3], M. N. Kozicki[1], M. J. Marinella[1], [1]Arizona State University, [2]Arizona State University,[3]Sandia National Laboratories*

P1-7 **A FeFET-Based Synapse Unit with Enhanced Current-Voltage Resolution for Low Power Sparse Neuromorphic Computing,** *X. Qin[1,3], S. Li[1,3], J. Li[1,3], X. Song[1,3], J. Zhang[2,3], D. Sun[1,3], C. Yu[1,3], Z. Zhou[1,3], X. Liu[1,3], J. Kang[1,3], [1]Peking University, [2]Peking University, [3]Beijing Advanced Innovation Center for Integrated Circuits*

P1-8 **ScAlN/AlGaN/GaN Ferroelectric HEMTs (FeHEMTs) for In-Memory Computing in Harsh Environments**, *J. Zhang, Y. Gan, J. Liu, Z. Fang, S. Mondal, Z. Mi, University of Michigan*

P1-9 **Improved Electrical and Reliability Characteristics of SiGe nGAAFET by Low Temperature Supercritical Fluid Condensation Technique**, *D.-B. Ruan[1], K.-S. Chang-Liao[1], H.-Y. Wang[1], G.-L. Luo[2], [1]National Tsing Hua University, [2]Taiwan Semiconductor Research Institute*

P1-10 **Wideband Phase-Programmable SOI CMOS Clock-Path IC**, *N. Jahan, California State University*

P1-11 **Positive Vth Tuning of In_2O_3 Top-Gate FET Based on Thermodynamics**, *S.-M. Chen[1], T. Hoshii[1], Y. Tsuruma[2], M. Sunagawa[2], S. Tomai[2], T. Takahashi[3], Y. Uraoka[3], K. Tsutsui[1], H. Wakabayashi[1], and K. Kakushima[1], [1]Institute of Science Tokyo, [2]Idemitsu Kosan Co., Ltd., [3]Nara Institute of Science and Technology*

P1-12 **Endurance Optimization of Reference and Data FeRAM Bitcells by Wear Leveling and Pattern-Adaptive Recovery,** *Y. Shen[1], Y. Zhu[1], J. Su[1], X. Zhang[1], H. Cai[1,2], Z. Fu[1,2], and J. Yang[1,2], [1]Southeast University, [2]National Center of Technology Innovation for EDA*

P1-13 **Evaluation of Novel MPB-based DRAM and FeRAM Dual-mode Memory**, *H.-H Chang[1], J.-Y. Lee[2], H. Liu[2], Y.-C. Chen[3], M.-H. Lee[2] and P. Su[3], [1]National Yang Ming Chiao Tung University, [2]National Taiwan University, [3]National Yang Ming Chiao Tung University*

P1-14 **Modification of Switching Kinetics on Ferroelectric AlScN Films by Electron Beam Irradiation**, *H. Nishida, S.-M. Chen, T. Hoshii, K. Tsutsui, H. Wakabayashi, and K. Kakushima, Institute of Science Tokyo*

P1-15 **Enhancing DRAM Performance via Epitaxial Silicon Plug Integration**, *P. Kumar, M. A. Lone, H. Raju and S. K. Manhas, Indian Institute of Technology Roorkee*

P1-16 **Stackable Dual Wordline DRAM Design Enabling Cell Performance Enhancement and Area Optimization,** *H. Raju, B. Fatima, P. Kumar, A. K. S. Chauhan and S. K. Manhas, Indian Institute of Technology Roorkee*

P1-17 **Achieving 36.8% Improvement in Circuit PPA Through Mixed-cell-height 2nm GAA CFET Cell Library,** *B.-H. Juan, P.-Y. Chu, L.-C. Huang, Z.-Y. Yu, T.-H. Chang, National Taiwan University*

P1-18 **Ensemble Monte Carlo Noise Analysis of a 2D Silicon PN Diode with SRH Recombination Using the Ramo–Shockley Theorem**, *S. S. Maram and C. E. Korman, The George Washington University*

P1-19 **Source-to-Drain Direct Tunneling Current Suppression Using Low Dielectric Constant MoS_2 Channel for Double-Gate Field-Effect Transistors**, *Y. Lu[1], S. Ueno[2], T. Hoshii[1], K. Kakushima[1], A. Hori[2] and H. Wakabayashi[2], [1]School of Engineering and [2]Institute of Integrated Research, Institute of Science Tokyo*

P1-20 **Comprehensive Cryogenic Modeling and Analysis of Back End of Line Interconnects for 3 nm GAAFET Technology**, *R. Saligram, University of Tennessee Knoxville*

P1-21 **Suppression of Parasitic Bipolar Junction Transistor Effect Using an Inner Amorphous Silicon Layer for High-Retention $4F^2$ Gate-All-Around DRAM**, *G.-B. Kim and M.-H. Baek, Kangwon National University*

P1-22 **Nanoscale InGaZnO Thin-Film Transistors Fabricated with Metal-Bridging-Free Scheme**, *M.-C. Yu[1], P.-W. Li[1], G.-W. Huang[2], and H.-C. Lin[1], [1]National Yang Ming Chiao Tung University, [2]Taiwan Semiconductor Research Institute*

P1-23 **Beyond Channel Scaling Limits: Planar Field Emission Devices Driven by Effective Work Function Engineering**, *Y.-H. Chen, H.-J. Chang, C.-T. Hsieh, T.-H. Chang, National Taiwan University*

P1-24 **Impact of Variations in Bond Angle Distortions Along Channel Thickness on Band Structure and Temperature-dependent I-V Behavior of Nanoscale Double Gate MOSFETs**, *Y. Dhote, S. Ghosh, S. Malla, A. K. Singh, A. S. Medury, Indian Institute of Science Education and Research Bhopal*

P1-25 **High-Performance InGaO TFTs by Optimizing Contact Resistance via an In_2O_3 Interlayer**, *C. Ye, P. Hong, J. Li, and X. Li, Huazhong University of Science and Technology*

P1-26 **Enhanced Thermal Gradients and Resulting Performance Degradation in MBCFETs Elevated Ambient Temperatures**, *E. S. Kim and S. Cho, Ewha Womans University*

P1-27 **Bias-Dependent Hole-Transmission Behavior and Schottky Barrier Modulation in Normally-off p-GaN HEMTs**, *C.-Y. Yang, D.-S. Chao, J.-H. Liang, National Tsing-Hua University*

P1-28 **Temperature-dependent Low-frequency Current Noise in Ge Quantum-dot/Si_3N_4-barrier Single-hole Transistors**, *C.-C. Lai, T. Tsai, H.-C. Lin, and P.-W. Li, National Yang Ming Chiao Tung University*